Abstract of the Disclosure

By suppressing a short- channel effect of a MIS field-effect transistor and reducing a fringing capacitance of a gate, a signal delay in the transistor can be shortened. The MIS field- effect transistor is formed d by forming a side- wall spacer from a dielectric having a large dielectric constant and then forming an impurity diffusion layer area with the side-wall spacer used as an introduction end in an ion implantation process to introduce impurities. In this case, the side wall of the side- wall spacer having the large dielectric constant has an optimum film thickness in the range from 5 nm to 15 nm, which is required for achieving a large driving current. On the other hand, a side- wall spacer on an outer side is made of a silicon- dioxide film, which is a dielectric having a small dielectric constant.